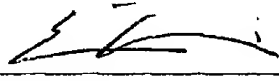




JC041 Rec'd PCT/PTO 25 MAY 2001

FORM PTO-1390 (REV 10-2000)		DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEYS DOCKET NUMBER 0819-559
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371			U.S. APPLICATION NO. (if known, see 37 CFR 1.5) 097856823
INTERNATIONAL APPLICATION NO. PCT/JP00/06851	INTERNATIONAL FILING DATE October 3, 2000	PRIORITY DATE CLAIMED October 4, 1999	
TITLE OF INVENTION METHOD FOR FABRICATING SEMICONDUCTOR DEVICE			
APPLICANT(S) FOR DO/EO/US Shin HASHIMOTO, Takenobu KISHIDA, Kyoko EGASHIRA, Yoshifumi HATA, Toru NISHIWAKI, Tomoya TANAKA			
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information: 1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371. 2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371. 3. <input checked="" type="checkbox"/> This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)). 4. <input checked="" type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (PCT Article 31). 5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2)) a. <input type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau). b. <input checked="" type="checkbox"/> has been communicated by the International Bureau. c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US). 6. <input checked="" type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)). 7. <input checked="" type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)). a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau). b. <input type="checkbox"/> have been communicated by the International Bureau. c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired. d. <input checked="" type="checkbox"/> have not been made and will not be made. 8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)). 9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). 10. <input type="checkbox"/> An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)). Items 11 to 16 below concern document(s) or information included: 11. <input type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98. 12. <input checked="" type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included. 13. <input checked="" type="checkbox"/> A FIRST preliminary amendment. <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment. 14. <input type="checkbox"/> A substitute specification. 15. <input type="checkbox"/> A change of power of attorney and/or address letter. 16. <input checked="" type="checkbox"/> Other items or information: Eight (8) Sheets of Formal Drawings			

J016 Rec'd PCT/PTO 25 MAY 2001

U.S. APPLICATION NO (If known, see 37 CFR 1.50) 09/856823		INTERNATIONAL APPLICATION NO PCT/JP00/06851		ATTORNEYS DOCKET NUMBER 0819-559	
17. <input checked="" type="checkbox"/> The following fees are submitted: BASIC NATIONAL FEE (37 CFR 1.492(a)(1) - (5)): Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO #1000.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO \$860.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(3)) paid to USPTO \$710.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) \$690.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) \$100.00 ENTER APPROPRIATE BASIC FEE AMOUNT =				CALCULATIONS	PTO USE ONLY
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				\$	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	16 - 20 =	0	X \$18.00	\$	
Independent claims	2 - 3 =	0	X \$80.00	\$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ \$270.00	\$270.00	
TOTAL OF ABOVE CALCULATIONS =				\$1,130.00	
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				\$	
SUBTOTAL =				\$1,130.00	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				\$	
TOTAL NATIONAL FEE =				\$1,130.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +				\$40.00	
TOTAL FEES ENCLOSED =				\$1,170.00	
				Amount to be refunded:	\$
				Charged:	\$
a. <input checked="" type="checkbox"/> A check in the amount of <u>\$1,170.00</u> to cover the above fees is enclosed. b. <input type="checkbox"/> Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed. c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. <u>19-2380</u> . A duplicate copy of this sheet is enclosed.					
NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.					
SEND ALL CORRESPONDENCE TO					
 SIGNATURE					
Eric J. Robinson NAME					
38,285 REGISTRATION NUMBER					

09/856623

J015 R&D PCT/JP 25 MAY 2001

Docket: 0819-559

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re New National Phase Patent Application of)
Shin HASHIMOTO et al.)
International Application No. PCT/JP00/06851) Attn: US/DO/EO
International Filing Date: October 3, 2000)
For: METHOD FOR FABRICATING)
SEMICONDUCTOR DEVICE) Date: May 25, 2001

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows: Please note that specification is presented below in its amended form. It is further presented as an Attachment to the Amendment whereby the amendments to the specification are outlined using the conventional method of bracketing and underlining.

Please amend the specification starting at page 17, line 23 through page 18, line 2 as follows:

Next, sputtering is carried out in a sputtering system having a chamber kept at a vacuum of 1×10^{-5} through 1×10^{-7} Pa, so as to deposit a metal film, such as a cobalt film 110, on the entire surface of the semiconductor substrate 100 as is shown in FIG. 3(c).

1978 1979 1980 1981 1982 1983 1984 1985 1986 1987 1988 1989 1990 1991 1992 1993 1994 1995 1996 1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041 2042 2043 2044 2045 2046 2047 2048 2049 2050 2051 2052 2053 2054 2055 2056 2057 2058 2059 2060 2061 2062 2063 2064 2065 2066 2067 2068 2069 2070 2071 2072 2073 2074 2075 2076 2077 2078 2079 2080 2081 2082 2083 2084 2085 2086 2087 2088 2089 2090 2091 2092 2093 2094 2095 2096 2097 2098 2099 2100 2101 2102 2103 2104 2105 2106 2107 2108 2109 2110 2111 2112 2113 2114 2115 2116 2117 2118 2119 2120 2121 2122 2123 2124 2125 2126 2127 2128 2129 2130 2131 2132 2133 2134 2135 2136 2137 2138 2139 2140 2141 2142 2143 2144 2145 2146 2147 2148 2149 2150 2151 2152 2153 2154 2155 2156 2157 2158 2159 2160 2161 2162 2163 2164 2165 2166 2167 2168 2169 2170 2171 2172 2173 2174 2175 2176 2177 2178 2179 2180 2181 2182 2183 2184 2185 2186 2187 2188 2189 2190 2191 2192 2193 2194 2195 2196 2197 2198 2199 2200 2201 2202 2203 2204 2205 2206 2207 2208 2209 2210 2211 2212 2213 2214 2215 2216 2217 2218 2219 2220 2221 2222 2223 2224 2225 2226 2227 2228 2229 2230 2231 2232 2233 2234 2235 2236 2237 2238 2239 2240 2241 2242 2243 2244 2245 2246 2247 2248 2249 2250 2251 2252 2253 2254 2255 2256 2257 2258 2259 2260 2261 2262 2263 2264 2265 2266 2267 2268 2269 2270 2271 2272 2273 2274 2275 2276 2277 2278 2279 2280 2281 2282 2283 2284 2285 2286 2287 2288 2289 2290 2291 2292 2293 2294 2295 2296 2297 2298 2299 2300 2301 2302 2303 2304 2305 2306 2307 2308 2309 2310 2311 2312 2313 2314 2315 2316 2317 2318 2319 2320 2321 2322 2323 2324 2325 2326 2327 2328 2329 2330 2331 2332 2333 2334 2335 2336 2337 2338 2339 2340 2341 2342 2343 2344 2345 2346 2347 2348 2349 2350 2351 2352 2353 2354 2355 2356 2357 2358 2359 2360 2361 2362 2363 2364 2365 2366 2367 2368 2369 2370 2371 2372 2373 2374 2375 2376 2377 2378 2379 2380 2381 2382 2383 2384 2385 2386 2387 2388 2389 2390 2391 2392 2393 2394 2395 2396 2397 2398 2399 2400 2401 2402 2403 2404 2405 2406 2407 2408 2409 2410 2411 2412 2413 2414 2415 2416 2417 2418 2419 2420 2421 2422 2423 2424 2425 2426 2427 2428 2429 2430 2431 2432 2433 2434 2435 2436 2437 2438 2439 2440 2441 2442 2443 2444 2445 2446 2447 2448 2449 2450 2451 2452 2453 2454 2455 2456 2457 2458 2459 2460 2461 2462 2463 2464 2465 2466 2467 2468 2469 2470 2471 2472 2473 2474 2475 2476 2477 2478 2479 2480 2481 2482 2483 2484 2485 2486 2487 2488 2489 2490 2491 2492 2493 2494 2495 2496 2497 2498 2499 2500 2501 2502 2503 2504 2505 2506 2507 2508 2509 2510 2511 2512 2513 2514 2515 2516 2517 2518 2519 2520 2521 2522 2523 2524 2525 2526 2527 2528 2529 2530 2531 2532 2533 2534 2535 2536 2537 2538 2539 2540 2541 2542 2543 2544 2545 2546 2547 2548 2549 2550 2551 2552 2553 2554 2555 2556 2557 2558 2559 2560 2561 2562 2563 2564 2565 2566 2567 2568 2569 2570 2571 2572 2573 2574 2575 2576 2577 2578 2579 2580 2581 2582 2583 2584 2585 2586 2587 2588 2589 2590 2591 2592 2593 2594 2595 2596 2597 2598 2599 2600 2601 2602 2603 2604 2605 2606 2607 2608 2609 2610 2611 2612 2613 2614 2615 2616 2617 2618 2619 2620 2621 2622 2623 2624 2625 2626 2627 2628 2629 2630 2631 2632 2633 2634 2635 2636 2637 2638 2639 2640 2641 2642 2643 2644 2645 2646 2647 2648 2649 2650 2651 2652 2653 2654 2655 2656 2657 2658 2659 2660 2661 2662 2663 2664 2665 2666 2667 2668 2669 2670 2671 2672 2673 2674 2675 2676 2677 2678 2679 2680 2681 2682 2683 2684 2685 2686 2687 2688 2689 2690 2691 2692 2693 2694 2695 2696 2697 2698 2699 2700 2701 2702 2703 2704 2705 2706 2707 2708 2709 2710 2711 2712 2713 2714 2715 2716 2717 2718 2719 2720 2721 2722 2723 2724 2725 2726 2727 2728 2729 2730 2731 2732 2733 2734 2735 2736 2737 2738 2739 2740 2741 2742 2743 2744 2745 2746 2747 2748 2749 2750 2751 2752 2753 2754 2755 2756 2757 2758 2759 2760 2761 2762 2763 2764 2765 2766 2767 2768 2769 2770 2771 2772 2773 2774 2775 2776 2777 2778 2779 2780 2781 2782 2783 2784 2785 2786 2787 2788 2789 2790 2791 2792 2793 2794 2795 2

N183028.1



REMARKS

The specification has been amended to correct minor informalities therein.

Examination on the merits is requested.

Respectfully submitted,

Sherman

Eric J. Robinson
Registration No. 38,285

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[illegible]

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend the specification starting at page 17, line 23 through page 18, line 2 as follows:

Next, sputtering is carried out in a sputtering system having a chamber kept at a vacuum of 1×10^{-5} through 1×10^{-7} Pa, so as to deposit a metal film, such as a cobalt film 110, on the entire surface of the semiconductor substrate 100 as is shown in FIG. 3(c).

Please amend the specification starting at page 28, line 21 through page 29, line 8 as follows:

Next, as is shown in FIG. 79a), after removing the silicon oxide film 209, the sputtering is carried out in a sputtering system having a chamber kept at a degree of vacuum of 1×10^{-5} through 1×10^{-7} Pa, thereby depositing a metal film, such as a cobalt film 211, on the entire surface of the semiconductor substrate 200. In this manner, similarly to Embodiment 2, cobalt atoms included in the cobalt film 211 are incorporated into the crystal lattice of silicon. Therefore, a nucleus of cobalt disilicide (CoSi_2) is formed on the interface between the n-type high concentration impurity layer 208 and the cobalt film 210, and a nucleus of cobalt disilicide (CoSi_2) is formed with respect to each crystal grain of the gate electrode 205.

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09/856823
JG19 Rec'd 25 MAY 2001

Description

METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

Technical Field

5 The present invention relates to a method for epitaxially growing a semiconductor-metal compound layer, in particular, a semiconductor-metal compound layer with high crystal orientation, in a surface portion of a semiconductor layer.

10

Background Art

15 In a semiconductor integrated circuit device required to be operated at a high speed, in accordance with recent refinement of semiconductor devices, increase in the sheet resistance and the contact resistance of a semiconductor layer including an impurity dispersed therein has become a serious problem.

20 As one means for overcoming this problem, a process for forming a silicide layer in a surface portion of the semiconductor layer has been proposed. A variety of metals have been proposed to be used for forming the silicide layer, among which a cobalt disilicide (CoSi_2) layer formed by using cobalt is regarded as a particularly promising silicide layer because it is good in both thermal stability and specific
25 resistance.

In the case where a surface portion of a silicon substrate is silicided by using cobalt, however, agglomeration can be caused in the cobalt silicide layer or a spike defect can be caused in the cobalt silicide layer during a reaction process occurring between cobalt atoms and silicon atoms (IEDM 1995-449, K. Goto). The agglomeration of the cobalt silicide layer leads to open circuit failure, and the occurrence of a spike defect leads to junction leakage.

As means for preventing the agglomeration and the occurrence of a spike defect in the cobalt silicide layer, a method for forming a cobalt silicide layer by epitaxial growth as follows is proposed in an article (Appl. Phys. Lett. 68, 1996, June). Specifically, the article proposes a technique of epitaxial growth of a cobalt silicide layer (oxide mediated epitaxy; OME) by forming a SiO_x ($x < 2$) film with a thickness of 0.5 through 1.5 nm on a semiconductor layer of silicon crystal, depositing a cobalt film in approximately several nm on the SiO_x film under ultra high vacuum and carrying out annealing for causing a reaction between cobalt atoms and silicon atoms. It is also described that the SiO_x film plays a role for promoting the growth of the cobalt silicide layer.

However, the aforementioned method for forming a cobalt silicide layer by the epitaxial growth requires ultra-high vacuum equipment for the deposition of a cobalt film, and the

ultra-high vacuum equipment is not employed in a general process for semiconductors of silicon. Therefore, this method is not suitable to the mass production process.

Furthermore, since the cobalt film is formed on the
5 SiO_x ($x < 2$) film having a very small thickness and including silicon excessively as compared with a stoichiometric composition, various problems occur in the aforementioned method due to variation in the film quality and the thickness of the SiO_x film. Specifically, in the case where a pin hole
10 is formed in the SiO_x film, cobalt and silicon are explosively reacted to each other through the pin hole, and hence, there arises a problem that the cobalt silicide layer cannot be epitaxially grown; and in the case where the thickness of the SiO_x film is fluctuated, the reaction
15 between the cobalt atoms and the silicon atoms is too rapidly proceeded in a portion with a small thickness, and hence, there arises a problem that the cobalt silicide layer cannot be satisfactorily epitaxially grown.

20

Disclosure of the Invention

In consideration of the aforementioned problems, an object of the invention is stably epitaxially growing a semiconductor-metal compound layer, such as a cobalt silicide layer, free from agglomeration and a spike defect under a
25 vacuum region or by using a fabrication system generally

employed in the semiconductor mass-production process.

In order to achieve the object, the present inventors have variously examined the causes of the agglomeration and a spike defect occurring in a cobalt silicide layer formed by the epitaxial growth, resulting in finding the following:

Thermodynamically, the mechanism for forming cobalt silicide through a reaction between cobalt atoms and silicon atoms is brought by proceeding a reaction, $\text{Co}_2\text{Si} \rightarrow \text{CoSi} \rightarrow \text{CoSi}_2$. In the reaction path of $\text{Co}_2\text{Si} \rightarrow \text{CoSi} \rightarrow \text{CoSi}_2$, however, the interface energy is so unstable and ununiform that cobalt silicide is polycrystallized, resulting in causing agglomeration and a spike defect.

Accordingly, the present inventors have concluded that CoSi_2 can be formed without passing through the reaction path of $\text{Co}_2\text{Si} \rightarrow \text{CoSi} \rightarrow \text{CoSi}_2$ by epitaxially growing the cobalt silicide layer after forming a seed layer of CoSi_2 on the interface between a semiconductor layer including silicon and a cobalt film.

Therefore, a variety of examination has been made on a method for forming a seed layer of CoSi_2 on the interface between the semiconductor layer including silicon and the cobalt film. As a result, it has been found that a seed layer of CoSi_2 can be formed by controlling the concentration of oxygen atoms present between the semiconductor layer and the cobalt film. Specifically, when a cobalt film is

deposited on a semiconductor layer including oxygen atoms distributed in a region in the vicinity of the surface, the amount of oxygen atoms sandwiched between the semiconductor layer and the cobalt film is decreased as compared with the
5 case where a SiO_x film is sandwiched between the semiconductor layer and the cobalt film. Therefore, the seed layer of CoSi_2 can be formed between the semiconductor layer and the cobalt film.

The present invention was devised on the basis of these
10 findings, and specifically, the first method for fabricating a semiconductor device of this invention comprises the steps of distributing a nonmetal element in a region in the vicinity of a surface portion of a semiconductor layer; depositing a metal film on the semiconductor layer; and
15 epitaxially growing a semiconductor-metal compound layer in the surface portion of the semiconductor layer by causing a reaction between an element included in the semiconductor layer and a metal included in the metal film through annealing carried out on the metal film.

20 In the first method for fabricating a semiconductor device of this invention, the metal film is deposited on the semiconductor layer after distributing the nonmetal element in the region in the vicinity of the surface portion of the semiconductor layer, and thereafter, the reaction between the
25 element included in the semiconductor layer and the metal

included in the metal film is caused by carrying out the annealing on the metal film. Therefore, the metal included in the metal film and the element included in the semiconductor layer can be avoided from too rapidly reacting
5 with each other, so as to prevent polycrystallization of the semiconductor-metal compound layer. Thus, according to the invention, a semiconductor-metal compound layer free from agglomeration and a spike defect can be stably formed under vacuum generally employed in the semiconductor mass
10 production process and at a low temperature.

In the first method for fabricating a semiconductor device, the step of distributing the nonmetal element preferably includes the steps of forming a compound layer including a semiconductor element and the nonmetal element on
15 the semiconductor layer; distributing the nonmetal element included in the compound layer in the region in the vicinity of the surface portion of the semiconductor layer through recoil by irradiating the compound layer with a particle energy beam; and removing the compound layer.

20 In this manner, the nonmetal element included in the compound layer can be definitely distributed in the region in the vicinity of the surface portion of the semiconductor layer through the recoil caused by the irradiation with the particle energy beam.

25 In the first method for fabricating a semiconductor

device, the step of distributing the nonmetal element preferably includes the steps of forming a compound layer including a semiconductor element and the nonmetal element on the semiconductor layer; and distributing the nonmetal element included in the compound layer in the region in the vicinity of the surface portion of the semiconductor layer through recoil and removing the compound layer by irradiating the compound layer with a particle energy beam.

In this manner, the nonmetal element included in the compound layer can not only be definitely distributed in the region in the vicinity of the surface portion of the semiconductor layer through the recoil caused by the irradiation with the particle energy beam, but also there is no need to conduct the step of removing the compound layer.

In these cases, a semiconductor layer having a face-centered cubic crystal structure, a semiconductor-metal compound layer having a face-centered cubic crystal structure and an amorphous compound layer can be used.

Also in these cases, the particle energy beam preferably includes a nonmetal element.

In this manner, the element included in the particle energy beam can be prevented from harmfully affecting the semiconductor layer.

In the first method for fabricating a semiconductor device, a semiconductor layer having a face-centered cubic

crystal structure and a semiconductor-metal compound layer having a face-centered cubic crystal structure can be used.

In the first method for fabricating a semiconductor device, a semiconductor layer having a diamond or zinc blende crystal structure and a semiconductor-metal compound layer having a calcium fluoride crystal structure can be used.

Preferably, in the first method for fabricating a semiconductor device, the semiconductor layer is a silicon layer, the nonmetal element is oxygen, the metal film is a cobalt film, and the semiconductor-metal compound layer is a cobalt silicide layer.

In this manner, a cobalt silicide layer that is thermally stable and has low sheet resistance can be definitely epitaxially grown in the surface portion of the semiconductor layer.

In this case, the oxygen preferably has a concentration of 4×10^{14} through $4 \times 10^{15} \text{ cm}^{-2}$.

In this manner, the reaction between cobalt atoms and silicon atoms can be satisfactorily proceeded, so that a cobalt silicide layer can be satisfactorily epitaxially grown in the surface portion of the silicon layer.

Also in this case, the step of distributing the nonmetal element preferably includes a step of forming a silicon oxide film on the silicon layer and distributing oxygen included in the silicon oxide film in the region in

the vicinity of the surface portion of the silicon layer by irradiating the silicon oxide film with the particle energy beam.

In this manner, oxygen atoms can be definitely distributed in the region in the vicinity of the surface portion of the silicon layer.

The second method for fabricating a semiconductor device of this invention comprises the steps of forming a gate electrode on a semiconductor layer; forming impurity layers on both sides of the gate electrode in the semiconductor layer; distributing a nonmetal element in a region in the vicinity of a surface portion of the semiconductor layer; depositing a metal film on the semiconductor layer; and epitaxially growing a semiconductor-metal compound layer in the surface portion of the semiconductor layer by causing a reaction between an element included in the semiconductor layer and a metal included in the metal film through annealing carried out on the metal film.

In the second method for fabricating a semiconductor device of this invention, a cobalt silicide layer that is thermally stable and has low sheet resistance and contact resistance can be formed in a surface portion of the semiconductor layer serving as a source or drain region, and a silicide layer with good quality can be formed in a surface

portion of the gate electrode. As a result, the performance of a semiconductor integrated circuit device including the MOSFET can be improved without increasing the number of fabrication procedures.

5 In the second method for fabricating a semiconductor device, the step of distributing the nonmetal element preferably includes the steps of forming a compound layer including a semiconductor element and the nonmetal element on the semiconductor layer; distributing the nonmetal element
10 included in the compound layer in the region in the vicinity of the surface portion of the semiconductor layer through recoil by irradiating the compound layer with a particle energy beam; and removing the compound layer.

In this manner, the nonmetal element included in the
15 compound layer can be definitely distributed in the region in the vicinity of the surface portion of the semiconductor layer through the recoil caused by the irradiation with the particle energy beam.

Preferably, in the second method for fabricating a
20 semiconductor device, the semiconductor layer is a silicon layer, the nonmetal element is oxygen, the metal film is a cobalt film, and the semiconductor-metal compound layer is a cobalt silicide layer.

In this manner, a cobalt silicide layer that is
25 thermally stable and has low sheet resistance can be

definitely epitaxially grown in the surface portion of the semiconductor layer.

In this case, the oxygen preferably has a concentration of 4×10^{14} through $4 \times 10^{15} \text{ cm}^{-2}$.

5 In this manner, the reaction between cobalt atoms and silicon atoms can be satisfactorily proceeded, so that the cobalt silicide layer can be satisfactorily epitaxially grown in the surface portion of the silicon layer.

10 Brief Description of Drawings

FIG. 1(a) is a diagram for showing the plane structure of a semiconductor device according to Embodiment 1.

FIG. 1(b) is a cross-sectional view taken on line Ib-Ib of FIG. 1(a).

15 FIGS. 2(a) through 2(c) are cross-sectional views for showing procedures in a method for fabricating a semiconductor device according to Embodiment 2.

FIGS. 3(a) through 3(c) are cross-sectional views for showing other procedures in the method for fabricating a
20 semiconductor device according to Embodiment 2.

FIGS. 4(a) and 4(b) are cross-sectional views for showing still other procedures in the method for fabricating a semiconductor device according to Embodiment 2.

FIGS. 5(a) through 5(c) are cross-sectional views for
25 showing procedures in a method for fabricating a

semiconductor device according to Embodiment 3.

FIGS. 6(a) through 6(c) are cross-sectional views for showing other procedures in the method for fabricating a semiconductor device according to Embodiment 3.

5 FIGS. 7(a) and 7(b) are cross-sectional views for showing still other procedures in the method for fabricating a semiconductor device according to Embodiment 3.

10 FIG. 8 is a characteristic diagram for showing the relationship between an oxygen concentration and the degree of epitaxial growth obtained by measuring the concentration of oxygen atoms by low energy SIMS.

Best Mode for Carrying Out the Invention

EMBODIMENT 1

15 A semiconductor device according to Embodiment 1 of the invention will now be described with reference to FIGS. 1(a) and 1(b).

20 FIG. 1(a) shows the plane structure of the semiconductor device of Embodiment 1 and FIG. 1(b) shows the cross-sectional structure taken on line Ib-Ib of FIG. 1(a).

The semiconductor device of Embodiment 1 may be any type of transistors including a CMOS transistor, a pMOS transistor and an nMOS transistor, and is herein described as an n-type MOS transistor.

25 As is shown in FIGS. 1(a) and 1(b), an n-type channel

stopper 11 is formed in a surface portion of a semiconductor substrate 10 of n-type silicon crystal having specific resistance of several $\Omega \cdot \text{cm}$, a field insulating film 13 serving as an isolation region is formed on the channel stopper 11, and a p-type well region 12 is formed in a portion of the semiconductor substrate 10 surrounded with the channel stopper 11.

In portions to be used as source and drain regions in the p-type well region 12, n-type low concentration impurity diffusion layers 16 and n-type high concentration impurity diffusion layers 18 having the LDD structure are formed. Also, on a portion of the semiconductor substrate 10 sandwiched between the source region and the drain region, a gate electrode 15 of a polysilicon film is formed with a gate insulating film 14 of a silicon oxide film sandwiched therebetween, and a sidewall 17 of a silicon oxide film is formed on the side face of the gate electrode 15.

As a characteristic of Embodiment 1, an epitaxially grown layer of cobalt disilicide (CoSi_2) is formed in a surface portion of the n-type high concentration impurity diffusion layer 18, and a polycrystalline cobalt disilicide layer is formed in a surface portion of the gate electrode 15 under conditions the same as those for growing the epitaxially grown layer on the n-type high concentration impurity diffusion layer 18 so as to have an epitaxial

relationship with each crystal grain of the polysilicon. The silicide layers formed in the surface portions of the n-type high concentration impurity diffusion layer 18 and the gate electrode 15 have a thickness of, for example, approximately 30 through 50 nm. Therefore, the resistance values of the n-type high concentration impurity diffusion layer 18 and the gate electrode 15 can be sufficiently lowered so as to improve the performance of a semiconductor integrated circuit device including the MOSFET of Embodiment 1.

10 An interlayer insulating film 22 is deposited on the semiconductor substrate 10, a metal interconnect 24 of, for example, an aluminum alloy film is formed on the interlayer insulating film 22, and the metal interconnect 24 is covered with a protection insulating film 25. The metal interconnect 15 24 is connected to the epitaxial silicide layer 21 formed in the surface portion of the n-type high concentration impurity diffusion layer 18 through a contact hole 23 formed in the interlayer insulating film 22. Therefore, the contact resistances of the n-type high concentration impurity 20 diffusion layer 18 and the metal interconnect 24 can be sufficiently lowered.

EMBODIMENT 2

A method for fabricating the semiconductor device of Embodiment 1 will now be described as Embodiment 2 of the 25 invention with reference to FIGS. 2(a) through 2(c), 3(a)

through 3(c), 4(a) and 4(b).

First, after forming a silicon oxide film with a small thickness on a semiconductor substrate 100 of n-type silicon crystal shown in FIG. 2(a), a silicon nitride film is deposited on the silicon oxide film. Thereafter, the silicon nitride film is patterned by the known photolithography technique and etching technique, so as to remove a portion of the silicon nitride film corresponding to a field insulating film region.

Next, with the patterned silicon nitride film used as a mask, an n-type impurity such as phosphorus and arsenic is ion implanted into the semiconductor substrate 100 at a high concentration, so as to form a channel stopper 101, and then, a p-type impurity such as boron is ion implanted into the semiconductor substrate 100, so as to form a p-type well region 102. Thereafter, the semiconductor substrate 100 is subjected to LOCOS for oxidizing a surface portion of the semiconductor substrate 100 not covered with the silicon nitride film through annealing, so as to form a field insulating film 103 with a thickness of, for example, 400 nm in the surface portion of the semiconductor substrate 100. The channel stopper 101 and the p-type well region 102 are activated through this annealing. Then, the silicon oxide film and the silicon nitride film are removed.

Next, a gate insulating film 104 of a silicon oxide

film with a thickness of, for example, 5 through 10 nm is formed on the entire surface of the semiconductor substrate 100 by, for example, thermal oxidation, a polysilicon film is deposited on the gate insulating film 104 by, for example, CVD, and the polysilicon film is patterned by the known photolithography technique and etching technique into a gate electrode 105.

Then, with the gate electrode 105 used as a mask, an n-type impurity such as arsenic and phosphorus is ion implanted into the semiconductor substrate 100 at a low concentration, so as to form an n-type low concentration impurity layer 106 as is shown in FIG. 2(b).

Subsequently, a silicon oxide film is deposited on the entire surface of the semiconductor substrate 100, and the silicon oxide film is subjected to anisotropic etching, so as to form a sidewall 107 on the side face of the gate electrode 105 as is shown in FIG. 2(c). Thereafter, with the gate electrode 105 and the sidewall 107 used as masks, an n-type impurity such as arsenic and phosphorus is ion implanted into the semiconductor substrate 100 at a high concentration, so as to form an n-type high concentration impurity layer 108. Then, the semiconductor substrate 100 is subjected to annealing, so as to active the n-type low concentration impurity layer 106 and the n-type high concentration impurity layer 108.

The sidewall 107 may be formed from a silicon nitride film instead of the silicon oxide film. Also, the annealing for activation may be carried out in first and second rapid thermal annealing processes described below.

5 Next, as is shown in FIG. 3(a), nonmetal element ions such as oxygen ions are ion implanted into the semiconductor substrate 100 at low acceleration energy of, for example, 100 through 500 eV, so that an oxygen atom distributed region 109 where oxygen atoms are distributed in a direction along the
10 substrate surface can be formed in the vicinity of the surface of the n-type high concentration impurity layer 108 and in the vicinity of the surface of the gate electrode 105 as is shown in FIG. 3(b). The oxygen atom distributed region 109 may be formed by, instead of the ion implantation of the
15 oxygen ions, plasma doping for distributing oxygen atoms.

 The depth for distributing the oxygen atoms of the oxygen atom distributed region 109 is preferably 0.5 through 5 nm from the surface of the n-type high concentration impurity layer 108 or the gate electrode 105, and the
20 concentration of the oxygen atoms included in the oxygen atom distributed region 109 is preferably $4 \times 10^{14} \text{ cm}^{-2}$ through $4 \times 10^{15} \text{ cm}^{-2}$. The reasons will be described later.

 Next, sputtering is carried out in a sputtering system having a chamber kept at a vacuum of 1×10^5 through 1×10^7
25 Pa, so as to deposit a metal film, such as a cobalt film 110,

on the entire surface of the semiconductor substrate 100 as is shown in FIG. 3(c).

The oxygen atom distributed region 109 is formed between the cobalt film 110 and the n-type high concentration impurity layer 108 or the gate electrode 105, and the oxygen atoms are distributed in a depth of 0.5 through 5 nm from the surface of the n-type high concentration impurity layer 108 or the gate electrode 105. Therefore, cobalt atoms included in the cobalt film 110 are prevented from diffusing into the semiconductor substrate 100 by the oxygen atom distributed region 109. Also, the crystal lattice of silicon present below the oxygen atom distributed region 109 can be seen from the cobalt atoms included in the cobalt film 110, and hence, even when a region above the oxygen atom distributed region 109 is disturbed by the ion implantation or the plasma doping, the reaction of the cobalt atoms is affected by the crystal structure of a region below the oxygen atom distributed region 109 of the semiconductor substrate 100. Therefore, a nucleus (not shown) of cobalt disilicide (CoSi_2) having a lattice constant matching to that of silicon crystal is formed on the interface between the n-type high concentration impurity layer 108 and the cobalt film 110. Furthermore, the gate electrode 105 is formed from polysilicon, and hence, a nucleus of cobalt disilicide (CoSi_2) is formed with respect to each crystal grain of the polysilicon in the same manner

as in the reaction between the cobalt atoms and the silicon atoms in the n-type high concentration impurity layer 108.

Next, the first rapid thermal annealing (RTA) is carried out for keeping the semiconductor substrate 100 at a temperature of 500°C for 10 seconds. Thus, the cobalt atoms included in the cobalt film 110 are diffused into the silicon region through the nucleus of cobalt disilicide and react with the silicon atoms. Therefore, as is shown in FIG. 3(c), an epitaxially grown layer (hereinafter referred to as a first epitaxial silicide layer) 111A of cobalt disilicide (CoSi_2) corresponding to the crystal structure of the previously formed nucleus of cobalt disilicide is formed in surface portions of the n-type high concentration impurity layer 108 and the gate electrode 105.

In the case where the cobalt film 110 has a thickness of 5 nm, the first epitaxial silicide layer 111A has a thickness of approximately 17 through 18 nm, and in the case where the cobalt film 110 has a thickness of 10 nm, the first epitaxial silicide layer 111A has a thickness of approximately 34 through 36 nm.

Furthermore, in the case where the semiconductor substrate 100 has a face-centered cubic crystal structure, the first epitaxial silicide layer 111A also has a face-centered cubic crystal structure, and in the case where the semiconductor substrate 100 has a diamond or zinc blende

crystal structure, the first epitaxial silicide layer 111A has a calcium fluoride (fluorite) crystal structure.

As described above, the oxygen atom distributed region 109 is formed in the regions at the depth of 0.5 through 5 nm from the surface in the vicinity of the surfaces of the n-type high concentration impurity layer 108 and the gate electrode 105, and hence, the cobalt atoms included in the cobalt film 110 are not directly in contact with the silicon atoms included in the n-type high concentration impurity layer 108 or the gate electrode 105. Therefore, the cobalt atoms and the silicon atoms are not reacted with each other too rapidly, so that agglomeration and polycrystallization of the first epitaxial silicide layer 111A can be avoided.

In the case where the concentration of the oxygen atoms included in the oxygen atom distributed region 109 is lower than $4 \times 10^{14} \text{ cm}^{-2}$, the cobalt atoms and the silicon atoms are too rapidly reacted with each other, so that there can be a fear of the agglomeration or the polycrystallization of the first epitaxial silicide layer 111A. On the other hand, in the case where the concentration of the oxygen atoms is higher than $4 \times 10^{15} \text{ cm}^{-2}$, a distance between the cobalt atoms and the crystal lattice of the semiconductor substrate 100 becomes too large to satisfactorily cause the reaction between the cobalt atoms and the silicon atoms. Accordingly, the concentration of the oxygen atoms included in the oxygen

atom distributed region 109 is preferably $4 \times 10^{14} \text{ cm}^{-2}$ through $4 \times 10^{15} \text{ cm}^{-2}$.

In the first epitaxial silicide layer 111A, all layers may be formed from cobalt disilicide (CoSi_2), or the lowermost layer (closer to the silicon layer) may be formed from cobalt disilicide (CoSi_2) with the uppermost layer (closer to the cobalt film 110) formed from cobalt silicide (CoSi). In the first epitaxial silicide layer 111A of Embodiment 2, the lowermost layer is formed from cobalt disilicide and the uppermost layer is formed from cobalt silicide. When a cobalt disilicide layer is formed at least on the interface with the silicon layer, the agglomeration of the cobalt silicide layer can be avoided, resulting in reducing a leakage current.

Next, as is shown in FIG. 4(a), a portion of the cobalt film 110 not reacted in the first rapid thermal annealing is removed by using an etchant of, for example, a mixture of an ammonia solution and hydrogen peroxide or a mixed acid solution including hydrochloric acid. Thereafter, the second rapid thermal annealing (RTA) is carried out for keeping the semiconductor substrate 100 at a temperature of 800°C for 10 seconds. Thus, the cobalt silicide included in the uppermost layer of the first epitaxial silicide layer 111A is also grown to cobalt disilicide, and hence, the first epitaxial silicide layer 111A is changed into a second epitaxial

silicide layer 111B in which all layers are formed from cobalt disilicide.

In the case where all the layers of the first epitaxial silicide layer 111A are formed from cobalt disilicide (CoSi_2), the second rapid thermal annealing can be omitted. In this case, the second epitaxial silicide layer 111B mentioned in the following description is read as the first epitaxial silicide layer 111A.

Next, as is shown in FIG. 4(b), an interlayer insulating film 112 of a silicon oxide film is deposited on the entire surface of the semiconductor substrate 100 by the CVD using, for example, TEOS (tetraethoxysilane), and a contact hole 113 is formed in the interlayer insulating film 112 by the known photolithography technique and etching technique.

Then, for example, an aluminum alloy film is deposited on the entire surface of the semiconductor substrate 100 so as to fill the contact hole 113 by, for example, the sputtering, and the aluminum alloy film is patterned by the known photolithography technique and etching technique into a metal interconnect 114. Thereafter, a protection insulating film 115 of a multi-layer film including, for example, a silicon oxide film and a silicon nitride film is deposited on the metal interconnect 114 by, for example, plasma CVD. Thus, the semiconductor device of Embodiment 1 is completed.

The metal interconnect 114 may be formed from, instead of the aluminum alloy film, a multi-layer film including an aluminum alloy film and a titanium nitride film or tungsten film.

5 According to Embodiment 2, the second epitaxial silicide layer 111B of cobalt disilicide is formed in the surface portions of the n-type high concentration impurity layer 108 and the gate electrode 105. Therefore, the sheet resistance of the n-type high concentration impurity layer
10 108 and the gate electrode 105 can be lowered to approximately $5 \Omega / \square$, which is much lower than the sheet resistance (of $100 \Omega / \square$) obtained without forming the second epitaxial silicide layer 111B. In addition, the contact resistance can be also lowered, so that the performance of a
15 semiconductor integrated circuit device including the MOSFET can be improved.

Furthermore, according to Embodiment 2, the metal film such as the cobalt film 110 is deposited after distributing the nonmetal element such as the oxygen atoms 109 in the
20 regions in the vicinity of the surfaces of the n-type high concentration impurity layer 108 and the gate electrode 105, and thereafter, the first and second rapid thermal annealing are carried out so as to form the second epitaxial silicide layer 111B of cobalt disilicide in the surface portions of
25 the n-type high concentration impurity layer 108 and the gate

electrode 105. Accordingly, the cobalt atoms and the silicon atoms are prevented from too rapidly reacting with each other, so that the agglomeration and the polycrystallization of the second epitaxial silicide layer 111B can be avoided and that
5 a spike defect can be prevented from being caused in the second epitaxial silicide layer 111B. As a result, disconnection derived from the agglomeration or the polycrystallization of the epitaxial silicide layer can be prevented as well as junction leakage derived from a spike
10 defect can be prevented.

Moreover, according to Embodiment 2, with the oxygen atoms 109 distributed in the regions in the vicinity of the surfaces of the n-type high concentration impurity layer 108 and the gate electrode 105, namely, with the oxygen atoms 109
15 present at a low concentration between the n-type high concentration impurity layer 108 or the gate electrode 105 and the cobalt film 110, the first rapid thermal annealing is carried out. Therefore, the first rapid thermal annealing can be carried out at a low temperature of, for example,
20 500°C.

Although the second epitaxial silicide layer 111B of cobalt disilicide is formed in the surface portions of both the n-type high concentration impurity layer 108 and the gate electrode 105 in Embodiment 2, the second epitaxial silicide
25 layer 111B may be formed in the surface portion of either the

n-type high concentration impurity layer 108 or the gate electrode 105 instead.

Although the oxygen atoms are distributed as the nonmetal element in the regions in the vicinity of the surfaces of the n-type high concentration impurity layer 108 and the gate electrode 105 in Embodiment 2, nitrogen atoms or fluorine atoms may be distributed instead of the oxygen atoms.

Although the cobalt film 110 is deposited as the metal film so as to form the second epitaxial silicide layer 111B of cobalt disilicide in Embodiment 2, a metal film of another transition metal such as nickel and iron may be deposited instead of the cobalt film 110, so as to form an epitaxial silicide layer from the transition metal included in the metal film and silicon.

EMBODIMENT 3

Another method for fabricating the semiconductor device of Embodiment 1 will now be described as Embodiment 3 of the invention with reference to FIGS. 5(a) through 5(c), 6(a) through 6(c), 7(a) and 7(b).

First, as is shown in FIG. 5(a), in the same manner as in Embodiment 2, a p-type well region 202 is formed by ion implanting a p-type impurity such as boron into a semiconductor substrate 200 of n-type silicon crystal, and then, a field insulating film 203 with a thickness of, for example, 400 nm is formed in a surface portion of the

semiconductor substrate 200 by the LOCOS. Subsequently, after a gate insulating film 204 of a silicon oxide film with a thickness of, for example, 5 through 10 nm is formed on the entire surface of the semiconductor substrate 200, a polysilicon film is deposited on the gate insulating film 204 by, for example, the CVD, and the polysilicon film is patterned into a gate electrode 205.

Next, with the gate electrode 205 used as a mask, an n-type impurity such as arsenic and phosphorus is ion implanted into the semiconductor substrate 200 at a low concentration, so as to form an n-type low concentration impurity layer 206 as is shown in FIG. 5(b).

Then, a silicon oxide film is deposited on the entire surface of the semiconductor substrate 200, and the silicon oxide film is subjected to the anisotropic etching, so as to form a sidewall 207 on the side face of the gate electrode 205 as is shown in FIG. 5(c). Thereafter, with the gate electrode 205 and the sidewall 207 used as masks, an n-type impurity such as arsenic and phosphorus is ion implanted into the semiconductor substrate 200 at a high concentration, so as to form an n-type high concentration impurity layer 208. Then, the semiconductor substrate 200 is subjected to annealing, thereby activating the n-type low concentration impurity layer 206 and the n-type high concentration impurity layer 208.

Then, as is shown in FIG. 6(a), a compound layer of a semiconductor element and a nonmetal film, such as a silicon oxide film 209, with a thickness of approximately 10 nm is formed on the entire surface of the semiconductor substrate 5 200.

The silicon oxide film 209 may be formed by any of the following methods: In the first method, a solution with oxidizing power (such as a mixed solution of ammonia, hydrogen peroxide and pure water) is supplied onto the 10 surface of the semiconductor substrate 200, thereby forming the so-called chemical oxide (SiO_2) film; in the second method, the semiconductor substrate 200 is exposed to oxygen plasma, thereby forming a silicon oxide film with a thickness of approximately 10 nm; and in the third method, the 15 semiconductor substrate 200 is heated to 750 through 900°C in an oxidizing atmosphere, thereby forming a thermally oxidized film with a thickness of approximately 10 nm.

Next, as is shown in FIG. 6(b), the silicon oxide film 209 is irradiated with a particle energy beam including a 20 nonmetal element, such as an Ar ion beam, at low energy. In this manner, owing to recoil of the particle energy beam, oxygen atoms included in the silicon oxide film 209 are distributed in a direction along the substrate surface in regions in the vicinity of the surfaces of the n-type high 25 concentration impurity layer 208 and the gate electrode 205,

so as to form an oxygen atom distributed region 210 as is shown in FIG. 6(c). In this case, the oxygen atoms included in the silicon oxide film 209 may be sputtered through the irradiation with the particle energy beam.

5 Also, the depth for distributing the oxygen atoms of the oxygen atom distributed region 210 is preferably 0.5 through 5 nm from the surface of the n-type high concentration impurity layer 208 or the gate electrode 205, and the concentration of the oxygen atoms in the oxygen atom
10 distributed region 210 is preferably $4 \times 10^{14} \text{ cm}^{-2}$ through $4 \times 10^{15} \text{ cm}^{-2}$. The reasons are the same as those described in Embodiment 2.

In the case where Ar ions are used for the irradiation of the particle energy beam, the peak of the distribution of
15 the oxygen atoms in the oxygen atom distributed region 210 is at a depth of 1 nm from the surface of the silicon region when the acceleration energy of the Ar ions is 100 eV, and the peak of the distribution of the oxygen atoms is at a depth of 2 nm from the surface of the silicon region when the
20 acceleration energy of the Ar ions is 300 eV.

Next, as is shown in FIG. 7(a), after removing the silicon oxide film 209, the sputtering is carried out in a sputtering system having a chamber kept at a degree of vacuum of 1×10^5 through 1×10^7 Pa, thereby depositing a metal
25 film, such as a cobalt film 211, on the entire surface of the

semiconductor substrate 200. In this manner, similarly to Embodiment 2, cobalt atoms included in the cobalt film 211 are incorporated into the crystal lattice of silicon. Therefore, a nucleus of cobalt disilicide (CoSi_2) is formed
5 on the interface between the n-type high concentration impurity layer 208 and the cobalt film 210, and a nucleus of cobalt disilicide (CoSi_2) is formed with respect to each crystal grain of the gate electrode 205.

Then, first rapid thermal annealing (RTA) is carried
10 out for keeping the semiconductor substrate 200 at a temperature of 500°C for 10 seconds, so as to form a first epitaxial silicide layer 212A in surface portions of the n-type high concentration impurity layer 208 and the gate electrode 205.

Since the oxygen atom distributed region 210 is formed
15 in the regions at the depth of 0.5 through 5 nm from the surface in the vicinity of the surfaces of the n-type high concentration impurity layer 208 and the gate electrode 205 in Embodiment 3, the cobalt atoms and the silicon atoms are
20 not too rapidly reacted with each other. Therefore, the agglomeration or polycrystallization of the first epitaxial silicide layer 212A can be avoided.

Now, a measurement result of the concentration of the oxygen atoms in the oxygen atom distributed region 210 will
25 be described.

FIG. 8 shows the result obtained by measuring the concentration of the oxygen atoms by low energy SIMS, in which the abscissa indicates the oxygen concentration (unit: number of atoms/cm²) and the ordinate indicates the degree of epitaxial growth. The degree of epitaxial growth can be expressed by intensity, and as the value of intensity is larger, the degree of epitaxial growth is larger. In this case, the ordinate indicates the peak intensity of CoSi₂ (400).

It is understood from the data shown in FIG. 8 at what concentration oxygen should be distributed in the vicinity of the surface of the semiconductor substrate 200 for forming the first epitaxial silicide layer 212A of cobalt disilicide (CoSi₂). Also, it is understood from FIG. 8 that cobalt disilicide can be epitaxially grown practically without causing a problem of heat resistance when the value on the ordinate is larger than 100. Specifically, as far as the value on the ordinate is larger than 100, cobalt disilicide can attain heat resistance against a high temperature of approximately 800°C, so as to avoid the agglomeration at a high temperature. The value on the ordinate is larger than 100 when the concentration of oxygen is 4×10^{14} cm⁻² through 4×10^{15} cm⁻².

Accordingly, when the concentration of the oxygen atoms in the oxygen atom distributed region 210 is controlled to be

4 × 10¹⁴ cm⁻² through 4 × 10¹⁵ cm⁻², the first epitaxial silicide layer 212A can be satisfactorily grown without causing the agglomeration of cobalt disilicide (CoSi₂).

In the first epitaxial silicide layer 212A, all layers may be formed from cobalt disilicide (CoSi₂), or the lowermost layer (closer to the silicon layer) may be formed from cobalt disilicide (CoSi₂) with the uppermost layer (closer to the cobalt film 110) formed from cobalt silicide (CoSi). In this manner, the agglomeration of the cobalt silicide layer can be prevented, resulting in reducing a leakage current.

Next, as is shown in FIG. 7(b), a portion of the cobalt film 211 not reacted in the first rapid thermal annealing is removed by using an etchant of, for example, a mixture of an ammonia solution and hydrogen peroxide or a mixed acid solution including hydrochloric acid. Thereafter, second rapid thermal annealing (RTA) is carried out for keeping the semiconductor substrate 200 at a temperature of 800°C for 10 seconds. Thus, the first epitaxial silicide layer 212A is changed into a second epitaxial silicide layer 212B in which all layers are formed from cobalt disilicide.

In the case where all the layers of the first epitaxial silicide layer 212A are formed from cobalt disilicide, the second rapid thermal annealing can be omitted. In this case, the second epitaxial silicide layer 212B mentioned in the

following description is read as the first epitaxial silicide layer 212A.

Thereafter, although not shown in the drawings, an interlayer insulating film, a contact hole, a metal
5 interconnect and a protection insulating film are formed in the same manner as in Embodiment 2. Thus, the semiconductor device of Embodiment 1 is completed.

According to Embodiment 3, the second epitaxial silicide layer 212B of cobalt disilicide is formed in the
10 surface portions of the n-type high concentration impurity layer 208 and the gate electrode 205. Therefore, the sheet resistance of the n-type high concentration impurity layer 208 and the gate electrode 205 can be lowered to approximately $5 \Omega/\square$, and the contact resistance can be also
15 lowered. As a result, the performance of a semiconductor integrated circuit device including the MOSFET can be improved.

Also, according to Embodiment 3, the particle energy beam is irradiated after depositing the silicon oxide film
20 209 on the semiconductor substrate 200. Therefore, the oxygen atoms 210 included in the silicon oxide film 209 can be definitely distributed in the regions in the vicinity of the surfaces of the n-type high concentration impurity layer 208 and the gate electrode 205.

25 Furthermore, the metal film such as the cobalt film 211

is deposited after the nonmetal element such as the oxygen atoms 210 is distributed in the regions in the vicinity of the surfaces of the n-type high concentration impurity layer 208 and the gate electrode 205, and then, the first and
5 second rapid thermal annealing are carried out so as to form the second epitaxial silicide layer 212B of cobalt disilicide in the surface portions of the n-type high concentration impurity layer 208 and the gate electrode 205. Therefore, the cobalt atoms and the silicon atoms are prevented from too
10 rapidly reacting with each other. As a result, the agglomeration or polycrystallization of the second epitaxial silicide layer 212B can be avoided as well as a spike defect can be prevented from being caused in the second epitaxial silicide layer 212B. In this manner, the disconnection
15 derived from the agglomeration or polycrystallization of the epitaxial silicide layer can be prevented as well as the junction leakage derived from a spike defect can be prevented.

Moreover, according to Embodiment 3, the first rapid thermal annealing is carried out with the oxygen atoms 210
20 distributed in the regions in the vicinity of the surfaces of the n-type high concentration impurity layer 208 and the gate electrode 205. Therefore, the first rapid thermal annealing can be carried out at a low temperature such as 500°C.

Although the second epitaxial silicide layer 212B of
25 cobalt disilicide is formed in the surface portions of both

the n-type high concentration impurity layer 208 and the gate electrode 205 in Embodiment 3, the second epitaxial silicide layer 212B may be formed in the surface portion of either the n-type high concentration impurity layer 208 or the gate electrode 205 instead.

Although the silicon oxide film 209 is formed on the semiconductor substrate 200 in Embodiment 3, a silicon nitride film or a silicon fluoride film may be deposited instead, so that nitrogen atoms or fluorine atoms can be distributed in the regions in the vicinity of the surfaces of the n-type high concentration impurity layer 208 and the gate electrode 205.

Although the cobalt film 211 is deposited as the metal film so as to form the second epitaxial silicide layer 212B of cobalt disilicide in Embodiment 3, a metal film of another transition metal such as nickel and iron may be deposited instead of the cobalt film 211, so as to form an epitaxial silicide layer from the transition metal included in the metal film and silicon.

20 MODIFICATION OF EMBODIMENT 3

In Embodiment 3, the silicon oxide film 209 is removed after distributing the oxygen atoms 210 in the regions in the vicinity of the surfaces of the n-type high concentration impurity layer 208 and the gate electrode 205 by irradiating the silicon oxide film 209 with the particle energy beam

including a nonmetal element such as the Ar ions. In contrast, in a modification of Embodiment 3, the mass and the energy of the particles included the particle energy beam, such as the Ar ions, are controlled, so that the silicon oxide film 209 can be removed through the irradiation with the particle energy beam in distributing the oxygen atoms 210 in the regions in the vicinity of the surfaces of the n-type high concentration impurity layer 208 and the gate electrode 205. In this manner, the procedure for removing the silicon oxide film 209 can be omitted.

Industrial Applicability

According to first or second method for fabricating a semiconductor device of this invention, rapid thermal annealing is carried out with a nonmetal element distributed in a region in the vicinity of the surface of a semiconductor layer, so as to cause a reaction between an element included in the semiconductor layer and a metal included in a metal film. Therefore, the metal included in the metal film and the element included in the semiconductor layer can be prevented from too rapidly reacting with each other. Accordingly, polycrystallization of an epitaxially grown semiconductor-metal compound layer can be avoided.

As a result, according to the invention, an epitaxially grown semiconductor-metal compound layer free from

[illegible]

CLAIMS

1. A method for fabricating a semiconductor device comprising the steps of:

5 distributing a nonmetal element in a region in the vicinity of a surface portion of a semiconductor layer;

depositing a metal film on said semiconductor layer; and

10 epitaxially growing a semiconductor-metal compound layer in the surface portion of said semiconductor layer by causing a reaction between an element included in said semiconductor layer and a metal included in said metal film through annealing carried out on said metal film.

2. The method for fabricating a semiconductor device of Claim 1,

15 wherein the step of distributing said nonmetal element includes the steps of:

forming a compound layer including a semiconductor element and said nonmetal element on said semiconductor layer;

20 distributing said nonmetal element included in said compound layer in the region in the vicinity of the surface portion of said semiconductor layer through recoil by irradiating said compound layer with a particle energy beam; and

25 removing said compound layer.

3. The method for fabricating a semiconductor device of Claim 1,

wherein the step of distributing said nonmetal element includes the steps of:

5 forming a compound layer including a semiconductor element and said nonmetal element on said semiconductor layer; and

10 distributing said nonmetal element included in said compound layer in the region in the vicinity of the surface portion of said semiconductor layer through recoil and removing said compound layer by irradiating said compound layer with a particle energy beam.

4. The method for fabricating a semiconductor device of Claim 2 or 3,

15 wherein said semiconductor layer has a face-centered cubic crystal structure,

 said semiconductor-metal compound layer has a face-centered cubic crystal structure, and

 said compound layer is amorphous.

20 5. The method for fabricating a semiconductor device of Claim 2 or 3,

 wherein said particle energy beam includes a nonmetal element.

25 6. The method for fabricating a semiconductor device of Claim 1,

wherein said semiconductor layer has a face-centered cubic crystal structure, and

said semiconductor-metal compound layer has a face-centered cubic crystal structure.

5 7. The method for fabricating a semiconductor device of Claim 1,

wherein said semiconductor layer has a diamond or zinc blende crystal structure, and

10 said semiconductor-metal compound layer has a calcium fluoride crystal structure.

8. The method for fabricating a semiconductor device of Claim 1,

wherein said semiconductor layer is a silicon layer,

said nonmetal element is oxygen,

15 said metal film is a cobalt film, and

said semiconductor-metal compound layer is a cobalt silicide layer.

9. The method for fabricating a semiconductor device of Claim 8,

20 wherein said oxygen has a concentration of 4×10^{14} through $4 \times 10^{15} \text{ cm}^{-2}$.

10. The method for fabricating a semiconductor device of Claim 8,

25 wherein the step of distributing said nonmetal element includes a step of forming a silicon oxide film on said

silicon layer and distributing oxygen included in said silicon oxide film in the region in the vicinity of the surface portion of said silicon layer by irradiating said silicon oxide film with the said particle energy beam.

5 11. A method for fabricating a semiconductor device comprising the steps of:

forming a gate electrode on a semiconductor layer;

forming impurity layers on both sides of said gate electrode in said semiconductor layer;

10 distributing a nonmetal element in a region in the vicinity of a surface portion of said semiconductor layer;

depositing a metal film on said semiconductor layer; and

15 epitaxially growing a semiconductor-metal compound layer in the surface portion of said semiconductor layer by causing a reaction between an element included in said semiconductor layer and a metal included in said metal film through annealing carried out on said metal film.

20 12. The method for fabricating a semiconductor device of Claim 11,

wherein the step of distributing said nonmetal element includes the steps of:

forming a compound layer including a semiconductor element and said nonmetal element on said 25 semiconductor layer;

distributing said nonmetal element included in
said compound layer in the region in the vicinity of the
surface portion of said semiconductor layer through recoil by
irradiating said compound layer with a particle energy beam;

5 and

removing said compound layer.

13. The method for fabricating a semiconductor device
of Claim 11,

10 wherein said semiconductor layer is a silicon layer,
said nonmetal element is oxygen,
said metal film is a cobalt film, and
said semiconductor-metal compound layer is a cobalt
silicide layer.

15 14. The method for fabricating a semiconductor device
of Claim 13,

wherein said oxygen has a concentration of 4×10^{14}
through $4 \times 10^{15} \text{ cm}^{-2}$.

[illegible]

5

Fig. 1(a)

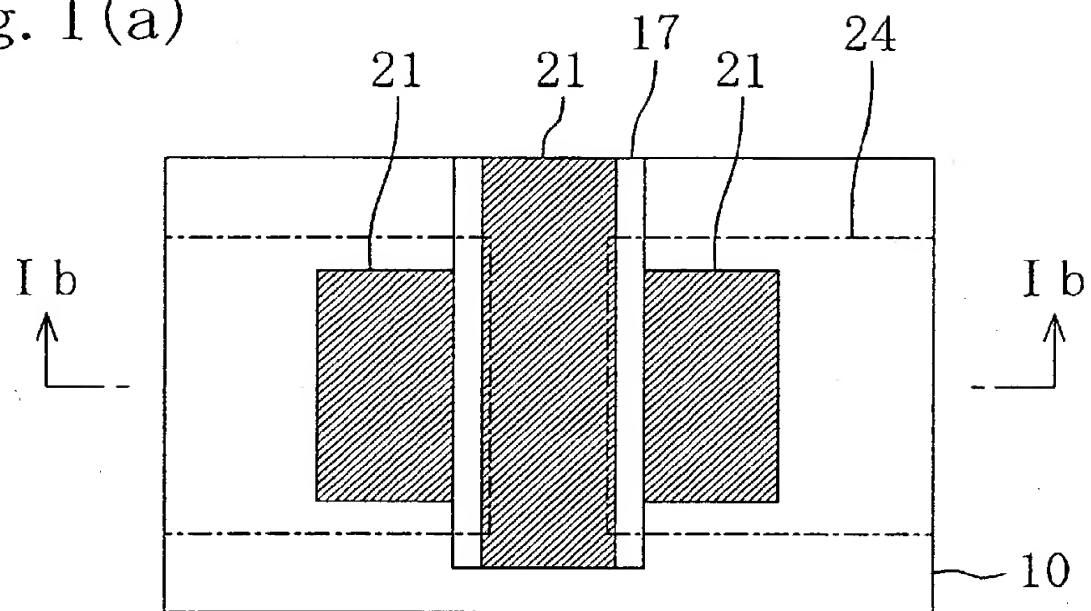


Fig. 1(b)

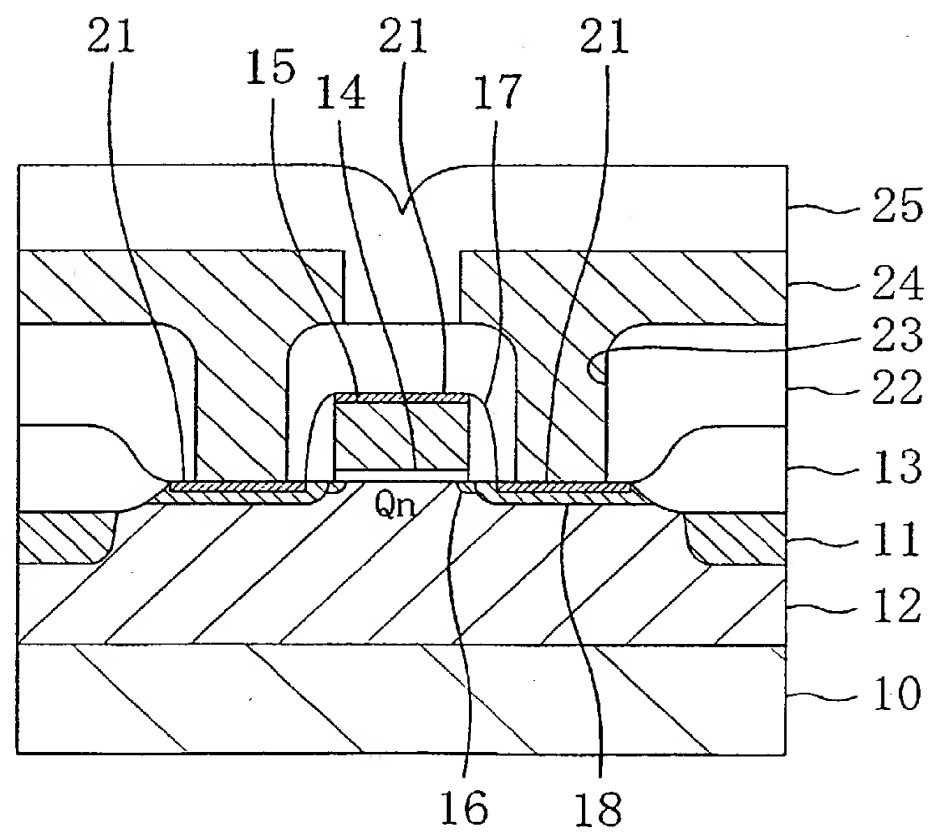


Fig. 2(a)

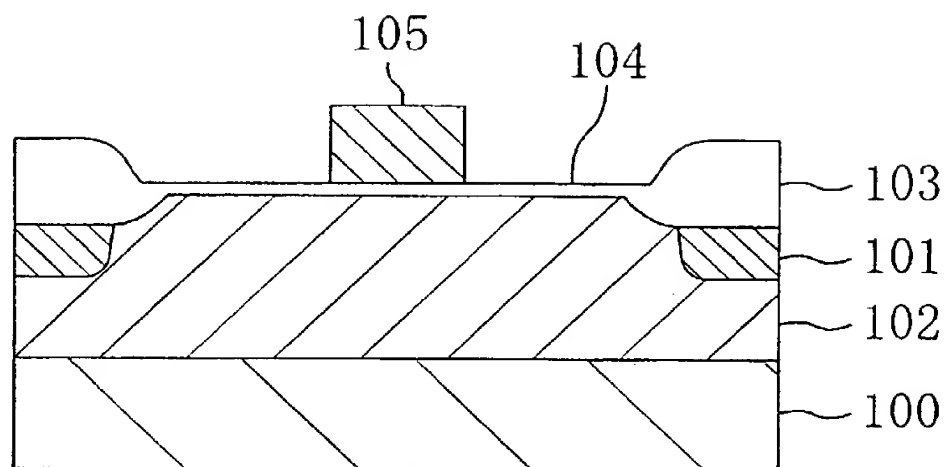


Fig. 2(b)

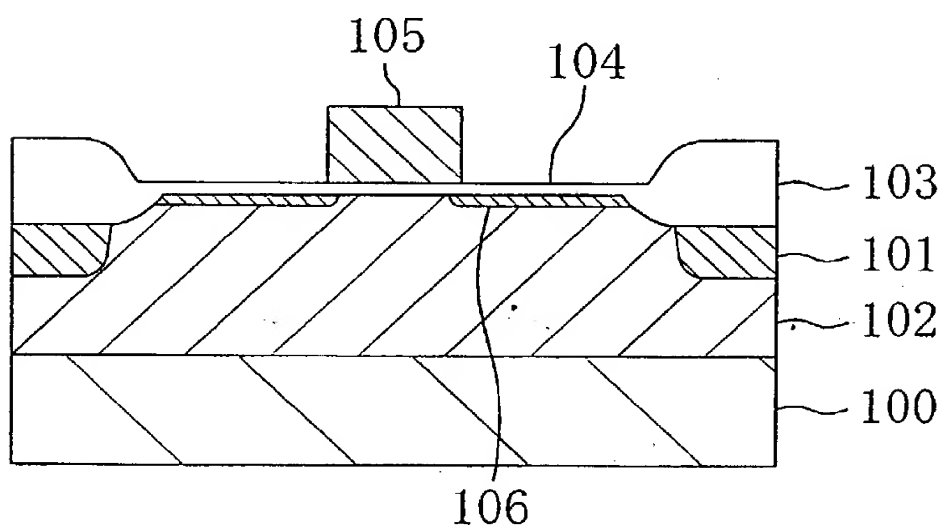


Fig. 2(c)

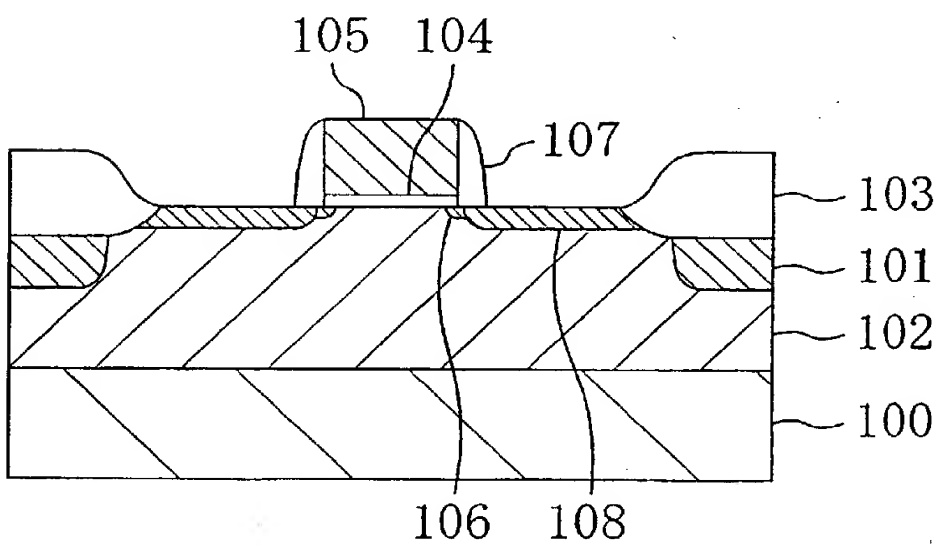


Fig. 3(a)

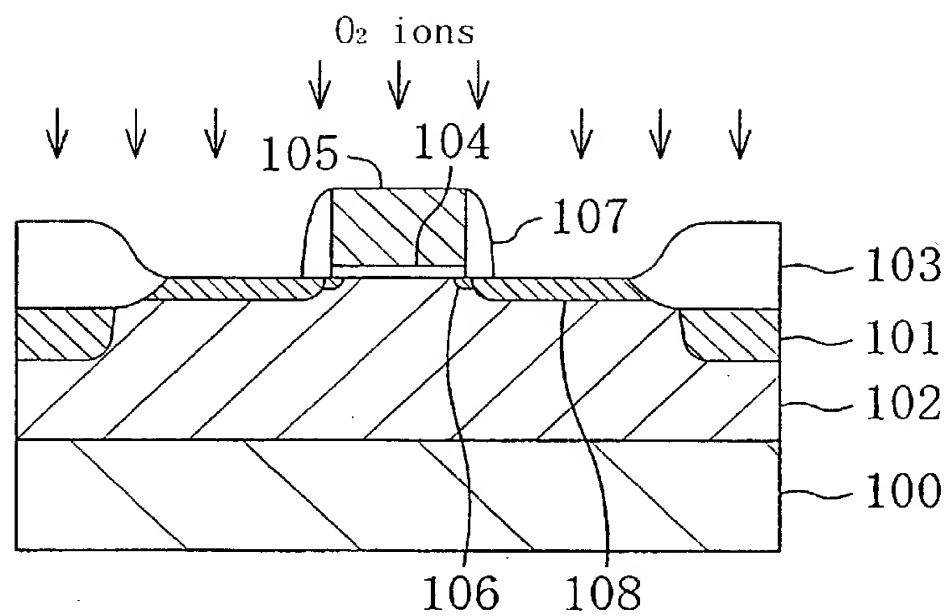


Fig. 3(b)

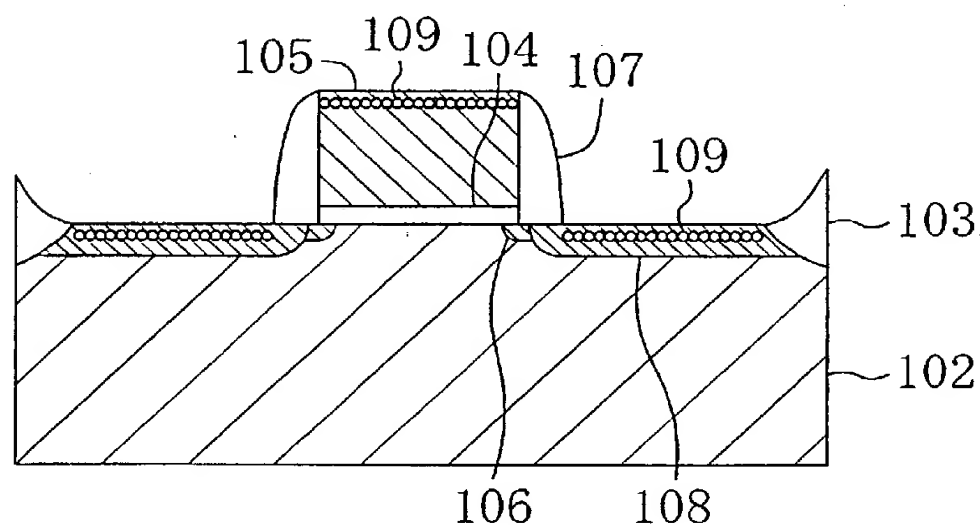


Fig. 3(c)

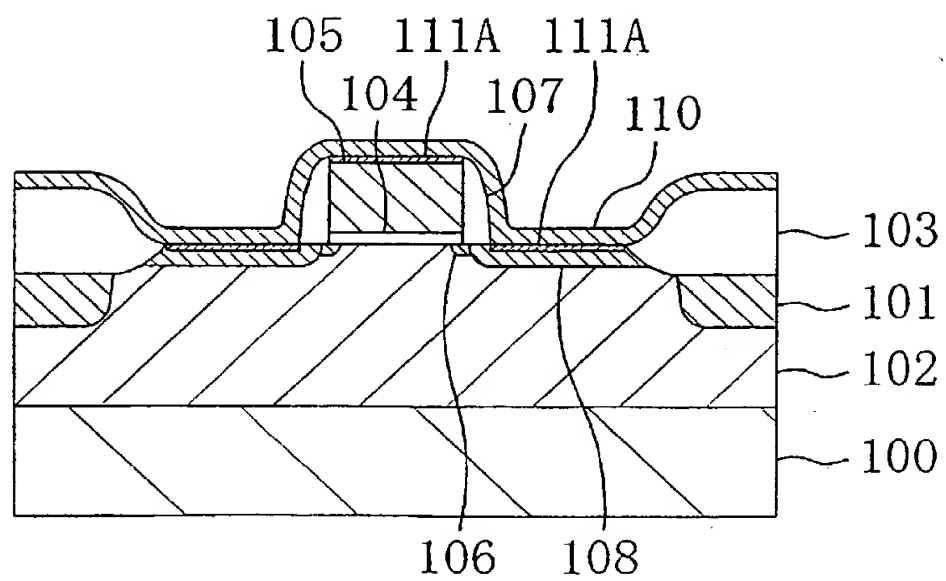


Fig. 4 (a)

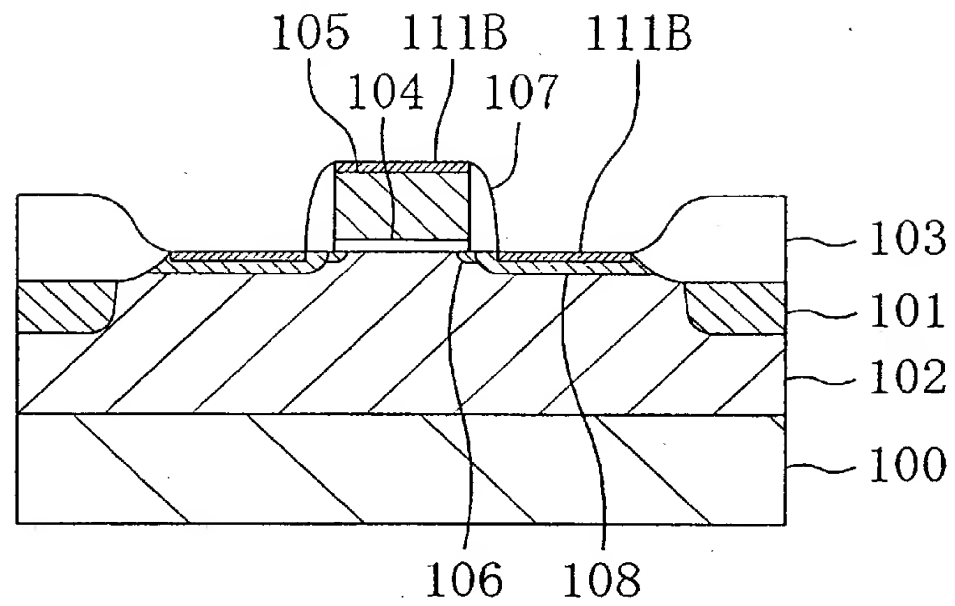
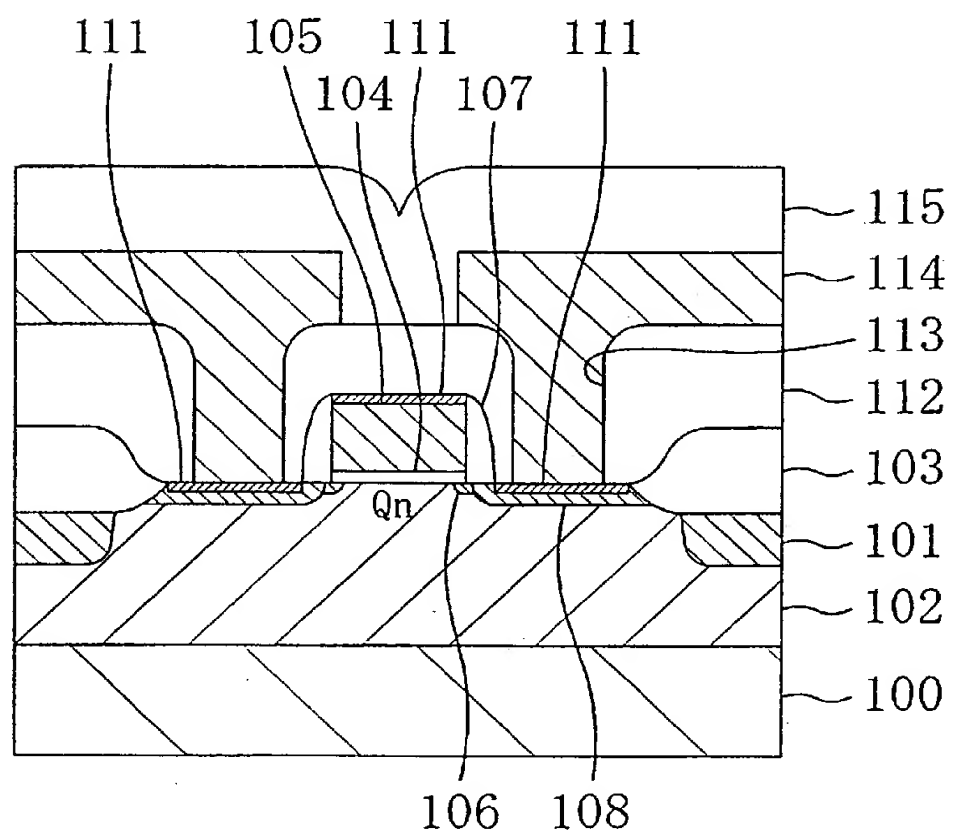


Fig. 4 (b)



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Fig. 5(a)

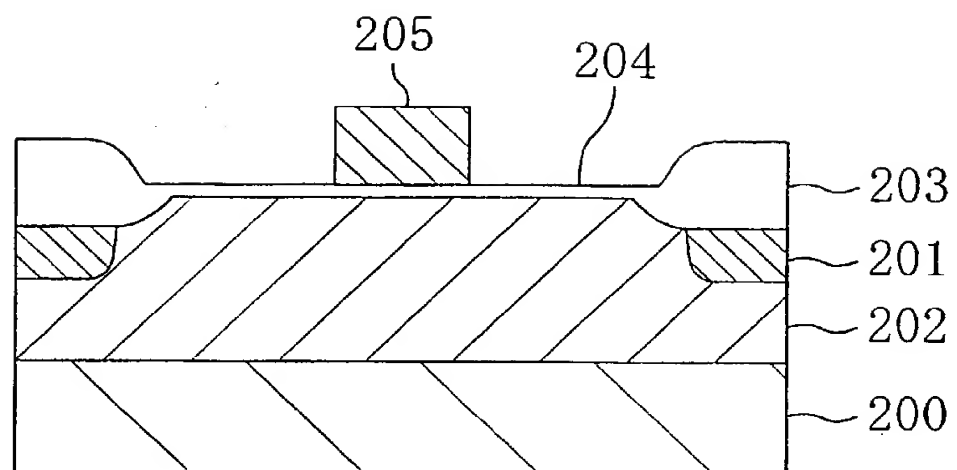


Fig. 5(b)

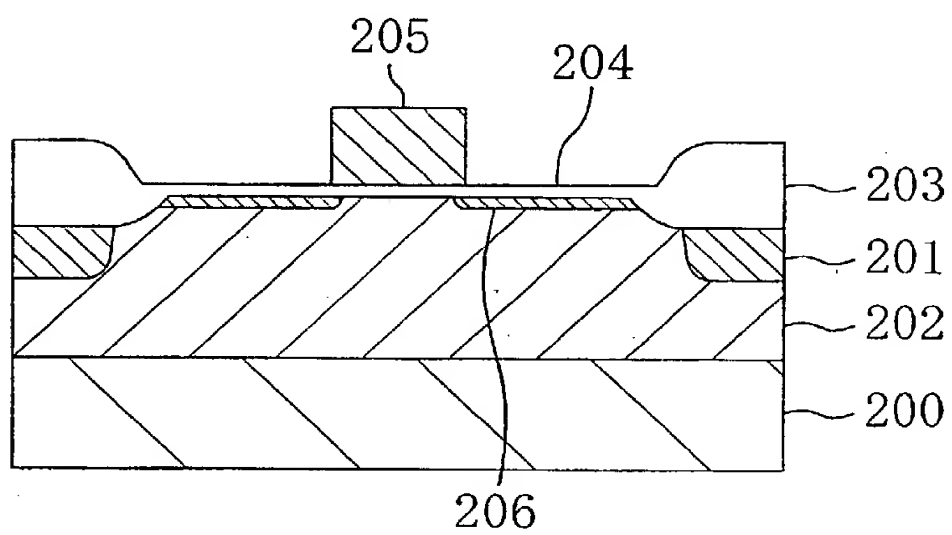
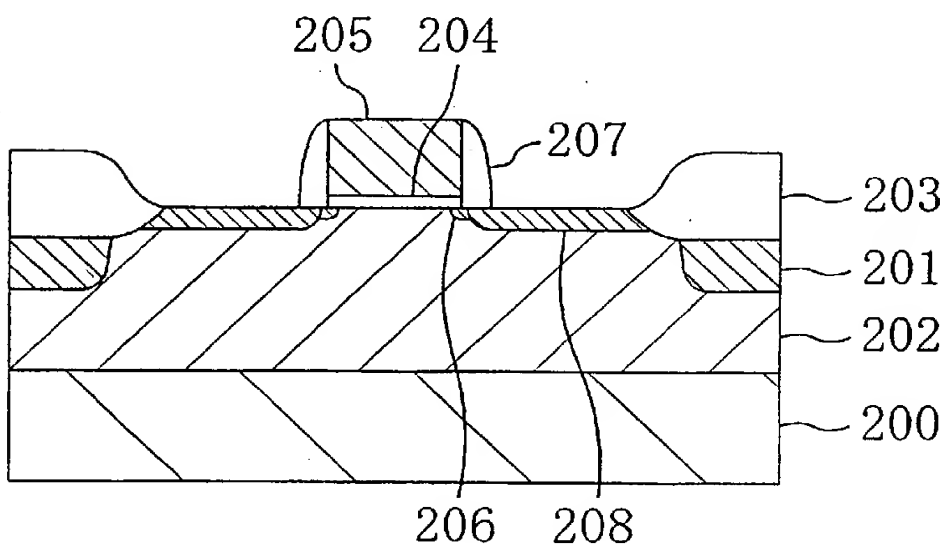


Fig. 5(c)



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Fig. 6(a)

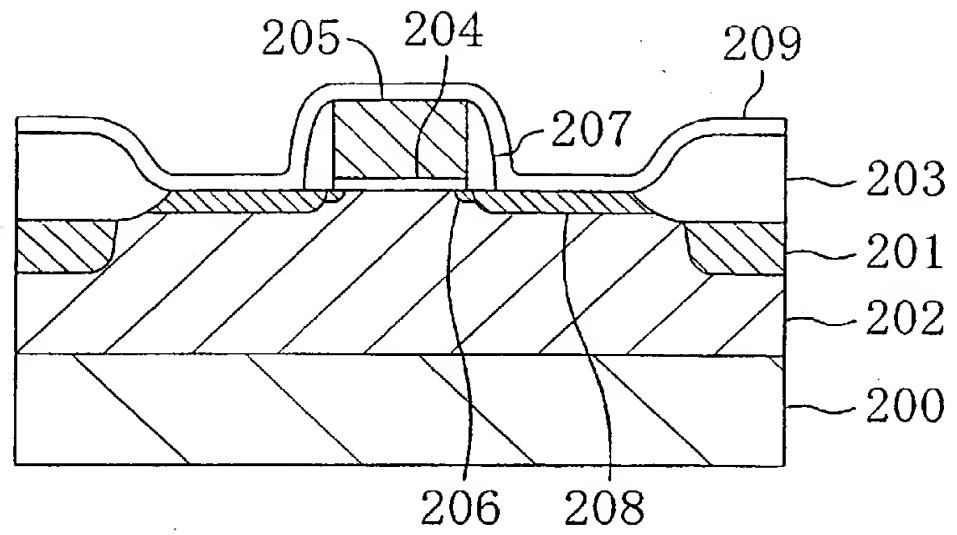


Fig. 6(b)

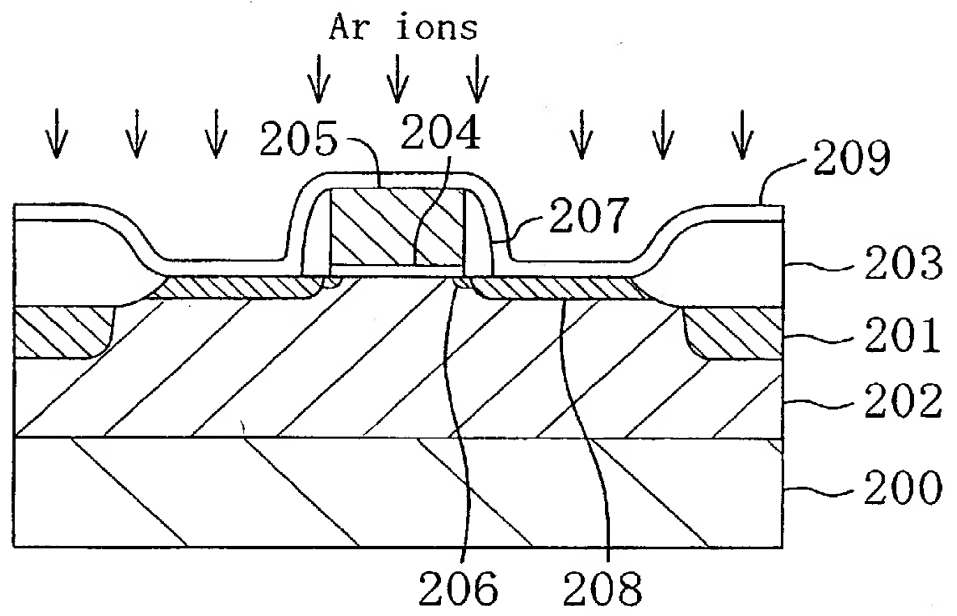


Fig. 6(c)

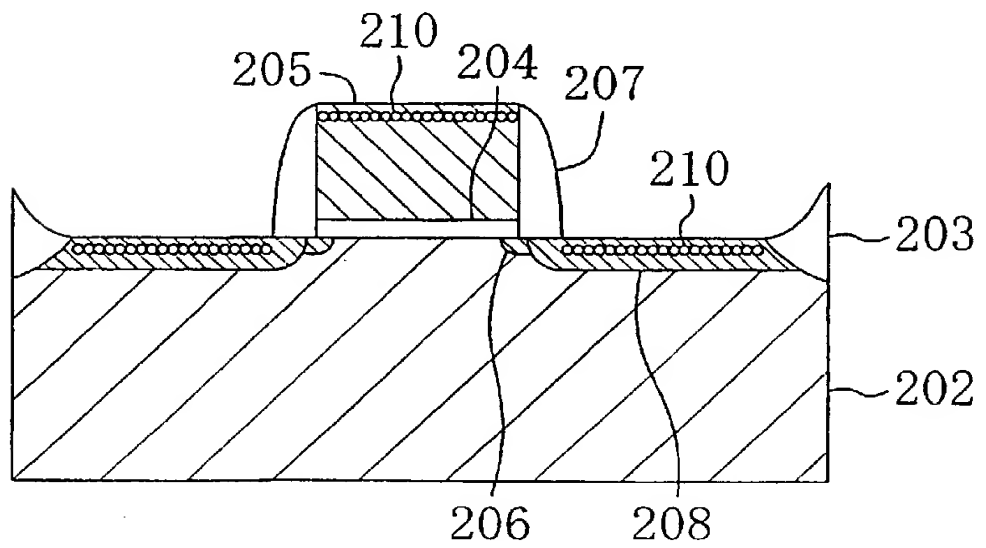


Fig. 7(a)

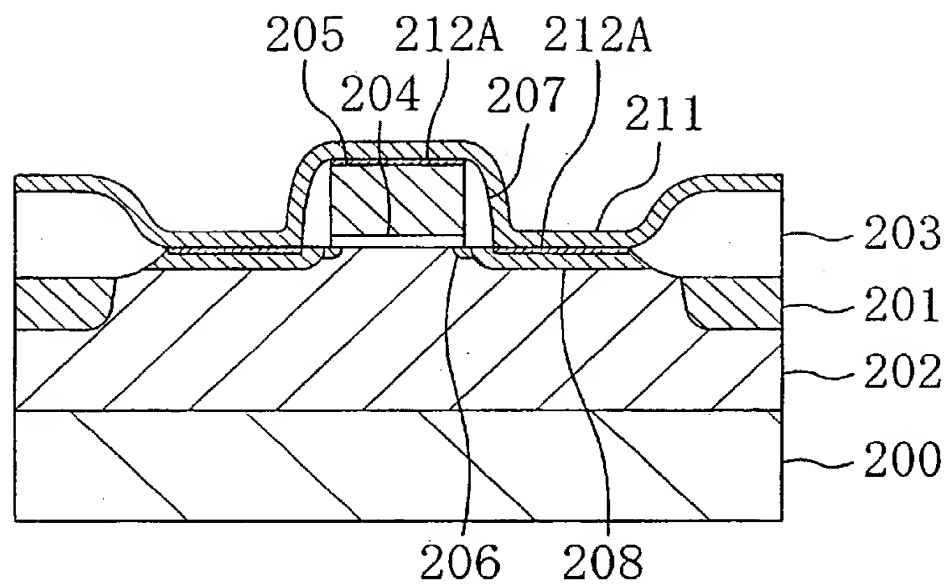


Fig. 7(b)

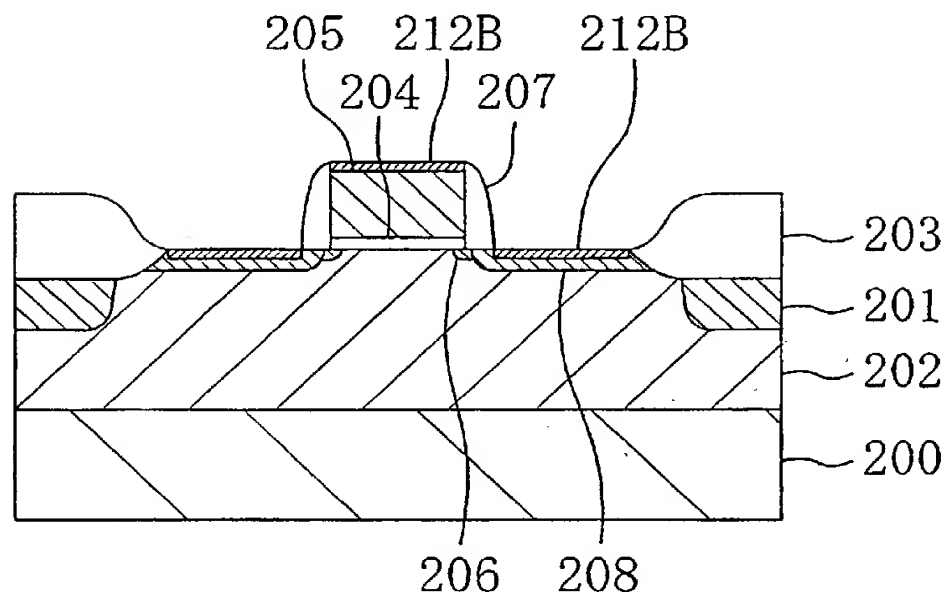
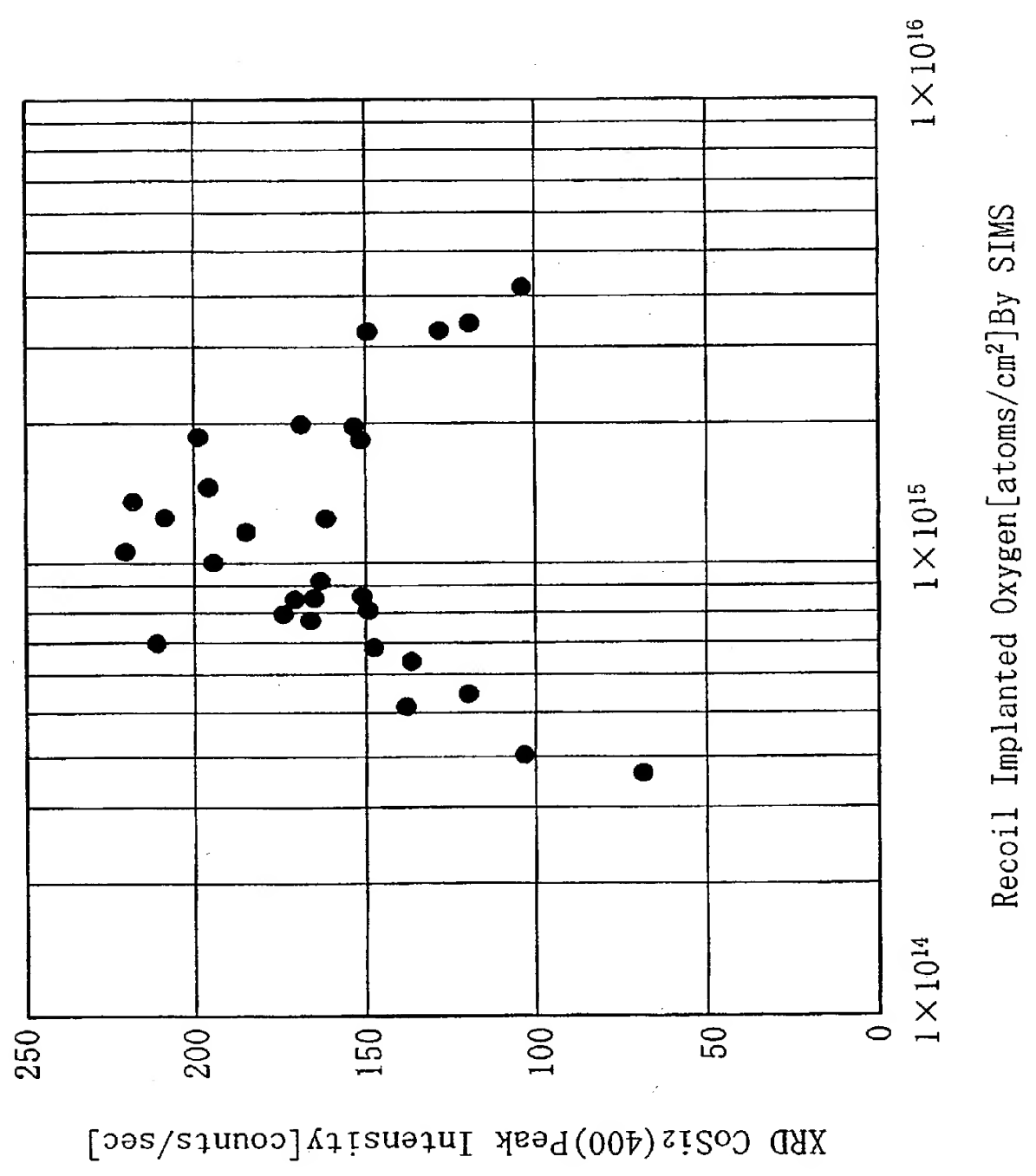


Fig. 8



COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY
(Includes Reference to PCT International Applications)

Attorney Docket No:

As a below named inventor, I hereby declare that:

My residence post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

the specification of which (check only one item below):

☐ is attached hereto.

☐ was filed as United States application

Serial No.

on

and was amended

on

(if applicable).

☒ was filed as PCT international application

Number **PCT/JP00/06851**

on **October 3, 2000**

and was amended under PCT Article 19

on

(if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations. § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international applications(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
Japan	11-282668	October 4, 1999	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
Japan	2000-263467	August 31, 2000	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO
			<input type="checkbox"/> YES <input type="checkbox"/> NO

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

(Includes Reference to PCT International Applications)

Attorney Docket No:

I hereby claim the benefit under Title 35, United States Code, § 119(c) or § 120, as applicable of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:

U.S. APPLICATIONS			STATUS (Check one)		
U.S. APPLICATION NUMBER	U.S. FILING DATE		PATENTED	PENDING	ABANDONED
PCT APPLICATIONS DESIGNATING THE U.S.					
PCT APPLICATION NO.	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED (if any)			

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The undersigned hereby authorize any U.S. attorney or agent named herein to accept and follow instructions from as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

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INVENTOR'S SIGNATURE

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POST OFFICE ADDRESS (Complete Address including City, State & Country)			